High-Speed UV-Erasable Programmable Logic Device

ATV750B

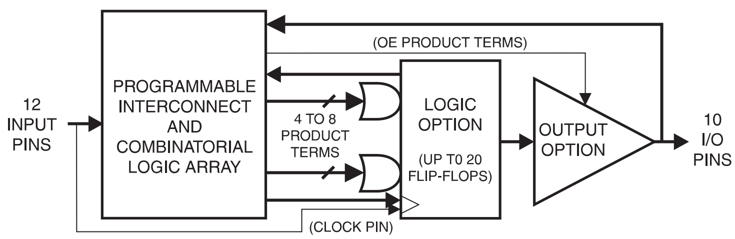
Features

- **Advanced, High-Speed Programmable Logic Device-Superset of 22V10**
  - **Improved Performance - 7.5 ns tPD, 95 MHz External Operation**
  - **Enhanced Logic Flexibility**
  - **Backward Compatible with ATV750/L Software and Hardware**
- **New Flip-Flop Features**
  - **D- or T-Type**
  - **Product Term or Direct Input Pin Clocking**
- **High-Speed Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**

Device	I_{CC}, Stand-By
ATV750B	125 mA
ATV750BL	15 mA

- **Highest Density Programmable Logic Available in a 24-Pin Package**
- **Increased Logic Flexibility**
  - **42 Array Inputs, 20 Sum Terms and 20 Flip-Flops**
- **Enhanced Output Logic Flexibility**
  - **All 20 Flip-Flops Feed Back Internally**
  - **10 Flip-Flops are Also Available as Outputs**
- **Full Military, Commercial and Industrial Temperature Ranges**

Logic Diagram



Description

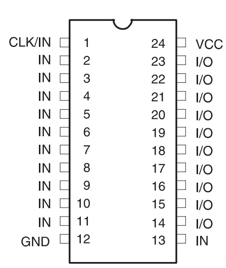
The ATV750Bs are twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High-speed logic and uniform, predictable delays guarantee fast in-system performance.

(continued)

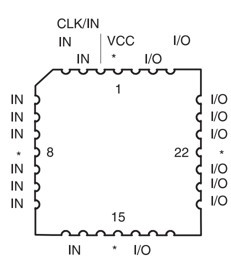
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
V_{CC}	+5V Supply

DIP/SOIC



PLCC/LCC



Top View

Rev. 0301D–05/98

Each of the ATV750B's 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

There are 171 total product terms available. A variable format is used to assign between four to eight product terms per sum term. There are two sum terms per output, providing added flexibility. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

The ATV750BL is a low power device with speeds as fast as 15 ns. The ATV750BL provides the optimum low power PLD solution, with full CMOS output levels. This device significantly reduces total system power, thereby allowing battery-powered operation.

Abosute Maximum Rating*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

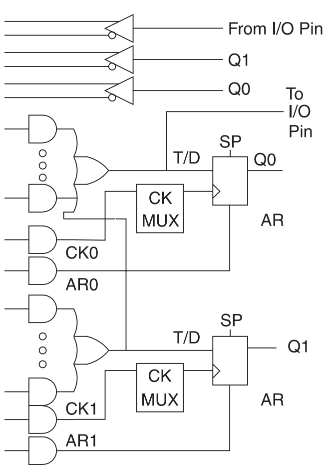
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

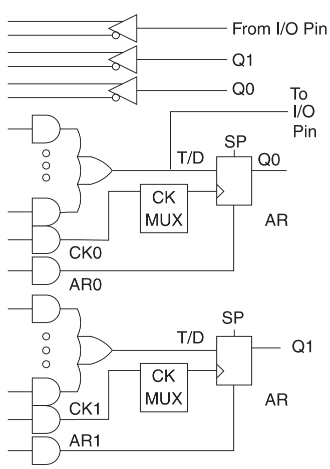
Logic Options

Combinatorial Output

Combined Terms

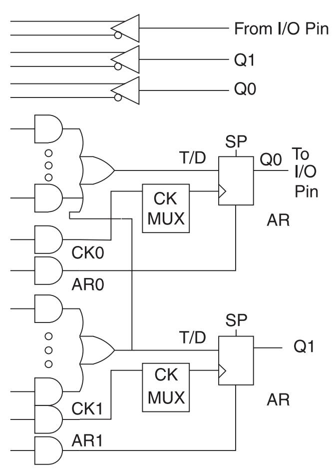


Separate Terms

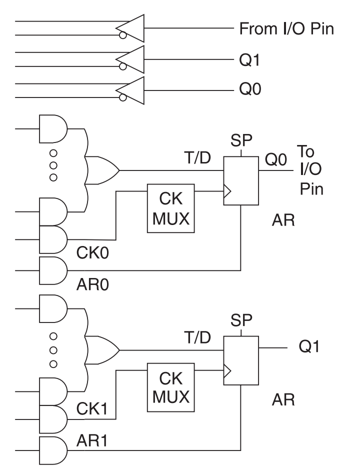


Registered Output

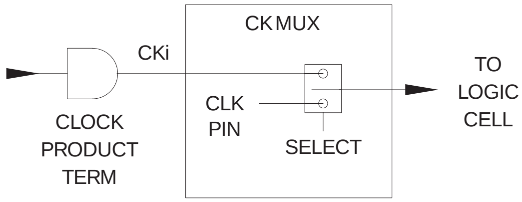
Combined Terms



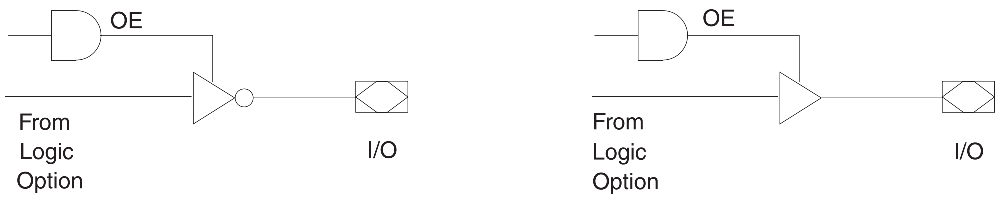
Separate Terms



Clock MUX



Output Options



DC and AC Operating Conditions(1)

	Commercial -7, -10, -15	Commercial -25	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

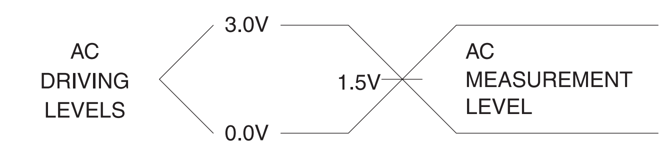
Note: 1. See ordering information for valid speed and temperature combination.

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		125	180	mA
				Ind.,Mil.		125	190	mA
			B-15, -25	Com.		125	180	mA
				Ind.,Mil.		125	190	mA
			BL-15	Com.		15	30	mA
				Ind.,Mil.		15	30	mA
I_{OS}(1)	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage	4.5 ≤ V_{CC} ≤ 5.5V			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			V

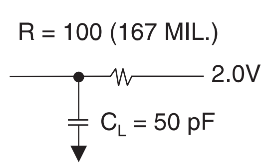
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

Input Test Waveforms and Measurement Levels

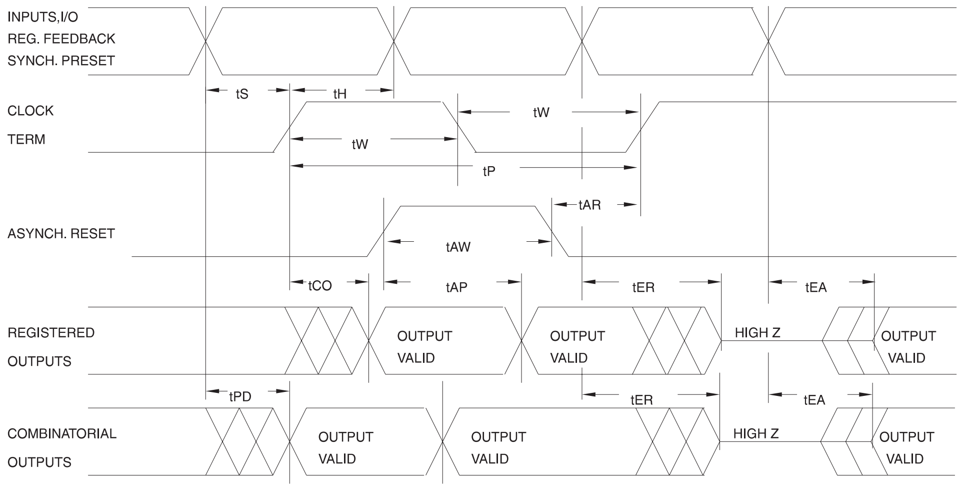


t_R, t_F < 3 ns (10% to 90%)

Output Test Load



AC Waveforms, Product Term Clock[1]



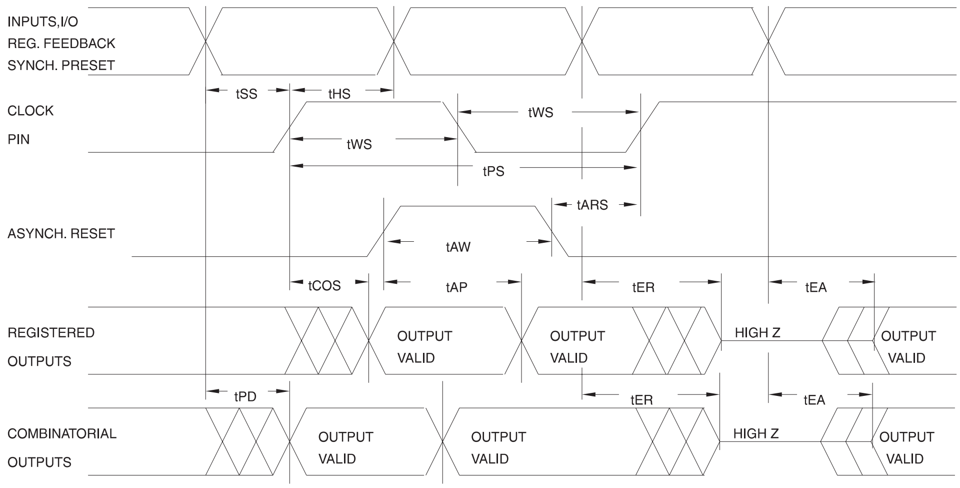
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics, Product Term Clock[1]

		-7		-10		B/BL-15		B/BL-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PD}	Input or Feedback to Non-Registered Output		7.5		10		15		25	ns
t_{EA}	Input to Output Enable		7.5		10		15		25	ns
t_{ER}	Input to Output Disable		7.5		10		15		25	ns
t_{CO}	Clock to Output	3	7.5	4	10	5	12	6	20	ns
t_{CF}	Clock to Feedback	1	5	4	7.5	5	9	5	10	ns
t_S	Input Setup Time	3		4		8/12		14		ns
t_{SF}	Feedback Setup Time	3		4		7		7		ns
t_H	Hold Time	1		2		5/7		5/7		ns
t_P	Clock Period	7		11		14		17		ns
t_W	Clock Width	3.5		5.5		7		8.5		ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$		95		71		50/41		29	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$		125		86		62		58	MHz
	No Feedback $1/(t_P)$		142		90		71		58	MHz
t_{AW}	Asynchronous Reset Width	5		10		15		20		ns
t_{AR}	Asynchronous Reset Recovery Time	3		10		15		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		8		12		15		25	ns
t_{SP}	Setup Time, Synchronous Preset	4		7		8		15		ns

Note: 1. See ordering information for valid part numbers.

AC Waveforms, Input Pin Clock[1]

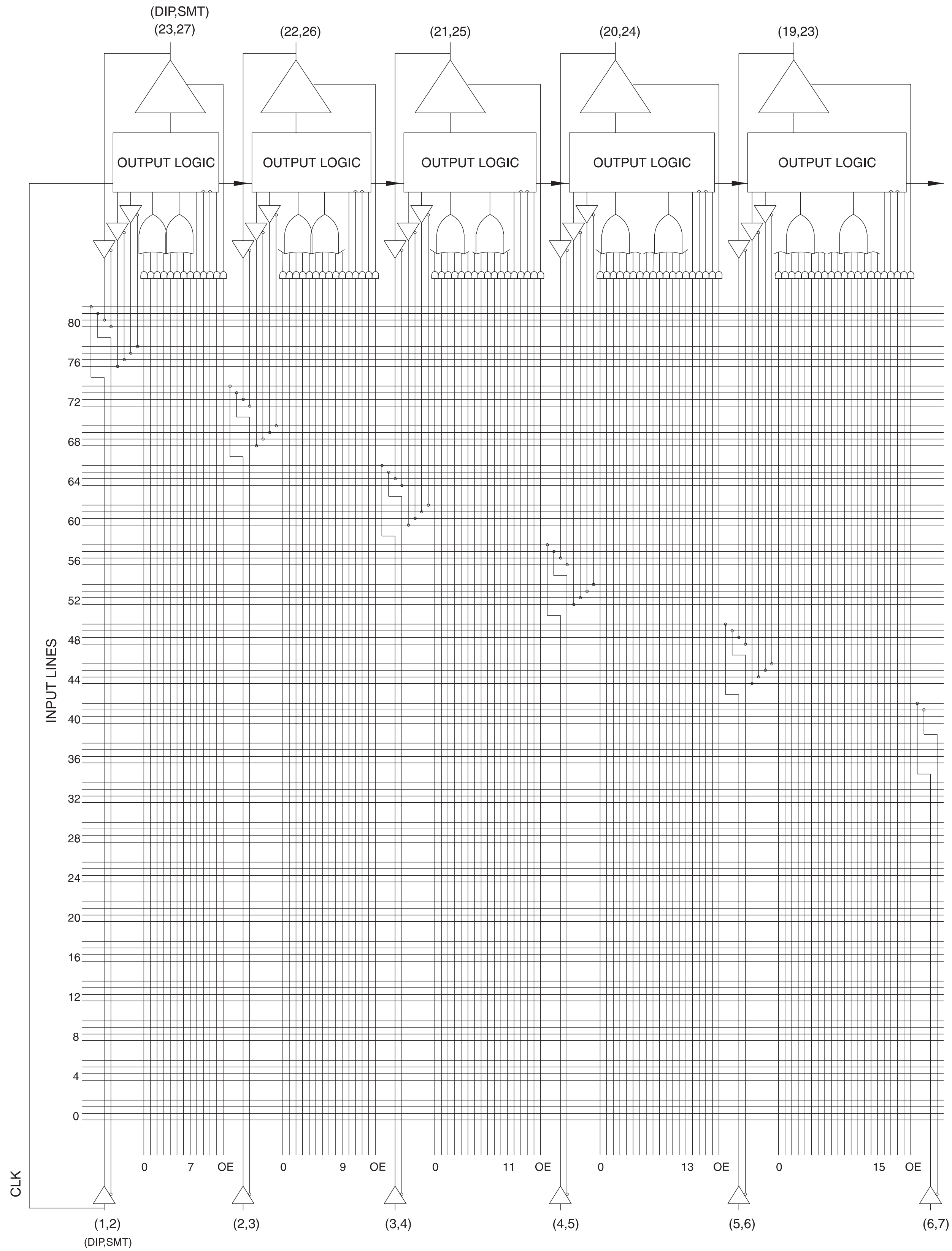


Notes: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

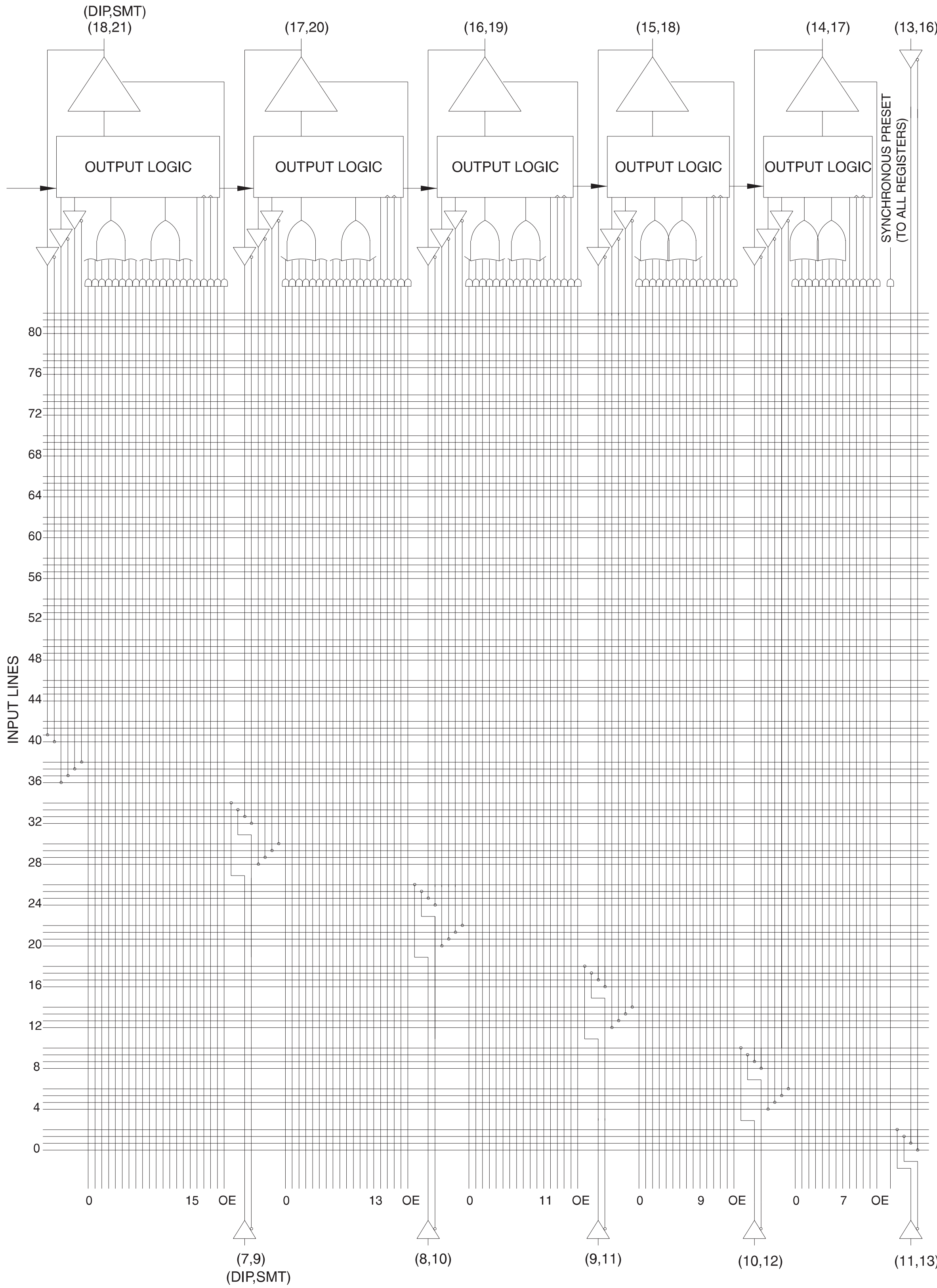
AC Characteristics, Input Pin Clock

Symbol	Parameter	-7		-10		B/BL -15		B/BL -25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		7.5		10		15		25	ns
t_{EA}	Input to Output Enable		7.5		10		15		25	ns
t_{ER}	Input to Output Disable		7.5		10		15		25	ns
t_{COS}	Clock to Output	0	6.5	0	7	0	6.5	0	12	ns
t_{CFS}	Clock to Feedback	0	3.5	0	5	0	5.5	0	7	ns
t_{SS}	Input Setup Time	4		5		8/12.5		9/15		ns
t_{SFS}	Feedback Setup Time	4		5		7		9		ns
t_{HS}	Hold Time	0		0		0		0		ns
t_{PS}	Clock Period	7		10		12		16		ns
t_{WS}	Clock Width	3.5		5		6		8		ns
F_{MAXS}	External Feedback $1/(t_{SS}+t_{COS})$		95		83		69/52		48/37	MHz
	Internal Feedback $1/(t_{SFS}+t_{CFS})$		133		100		80		62	MHz
	No Feedback $1/(t_{PS})$		142		100		83		62	MHz
t_{AW}	Asynchronous Reset Width	5		10		15		20		ns
t_{ARS}	Asynchronous Reset Recovery Time	5		10		15		25		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		8		10		15		25	ns
t_{SPS}	Setup Time, Synchronous Preset	5		5/9		11		15		ns

Functional Logic Diagram ATV750B, Upper Half

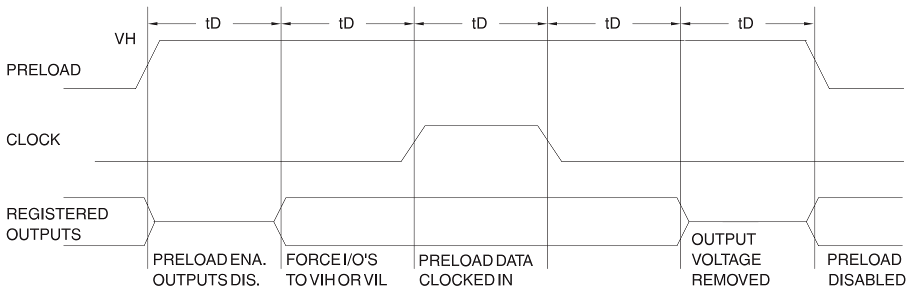


Functional Logic Diagram ATV750B, Lower Half



Preload of Registered Outputs

The ATV750B's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the output polarity. The PRELOAD state is entered by placing a 10.25V to 10.75V signal on pin 8 on DIPs, and lead 10 on SMDs. When the clock term is pulsed high, the data on the I/O pins is placed into the register chosen by the Select Pin.



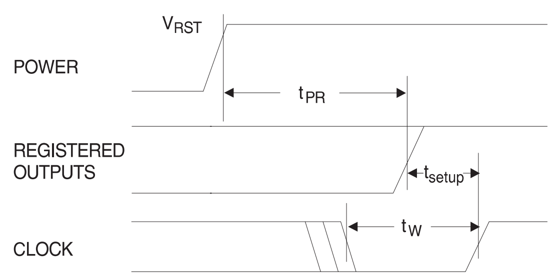
Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #0 State after cycle	Register #1 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power Up Reset

The registers in the ATV750Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock terms or pin high, and
3. The clock pin, or signals from which clock terms are derived, must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Pin Capacitance

f = 1 MHz, T = 25°C(1)

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Using the ATV750B's Many Advanced Features

The ATV750B's advanced flexibility packs more usable gates into 24-pins than any other logic device. The ATV750Bs start with the popular 22V10 architecture, and add several enhanced features:

- **Selectable D- and T-Type Registers -** Each ATV750B flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Selectable Asynchronous Clocks -** Each of the ATV750B's flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Full Bank of Ten More Registers -** The ATV750B provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.
- **Independent I/O Pin and Feedback Paths -** Each I/O pin on the ATV750B has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

Programming Software Support

As with all other Atmel PLDs, several third party development software products support the ATV750Bs. Several third party programmers support the ATV750B as well. Additionally, the ATV750B may be programmed to perform the ATV750/L's functional subset (no T-type flip-flops or pin clocking) using the ATV750/L JEDEC file. In this case, the ATV750B becomes a direct replacement or speed upgrade for the ATV750/L. The ATV750/L programming algorithm is different from the ATV750B algorithm. Choose the appropriate device in your programmer menu to ensure proper programming. Please refer to the *Programmable Logic Development Tools* section for a complete PLD software and programmer listing.

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750B. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750B fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

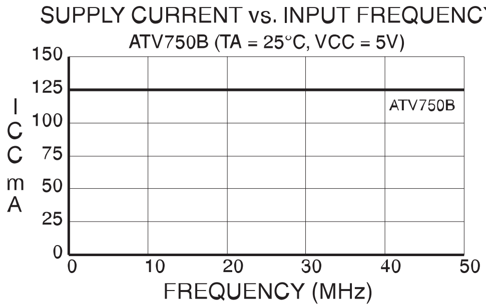
Erasure Characteristics

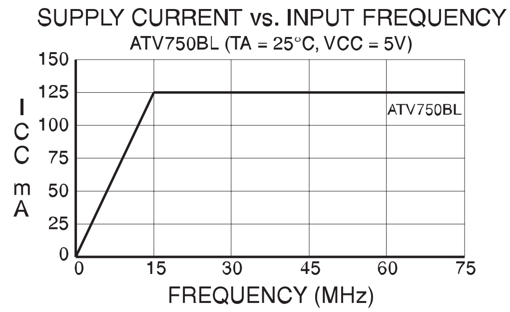
The entire memory array of an ATV750B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

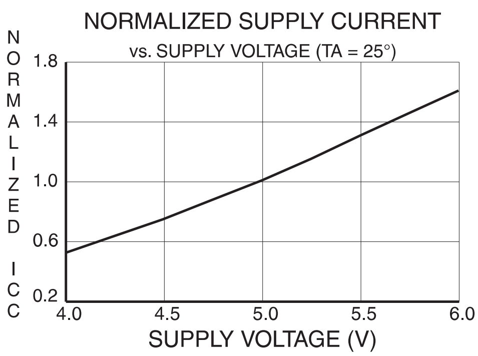
Atmel CMOS PLDs

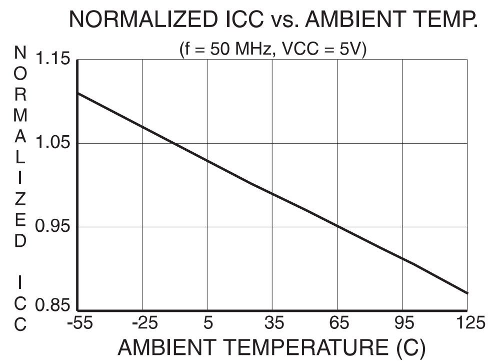
The ATV750B utilizes an advanced 0.65-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

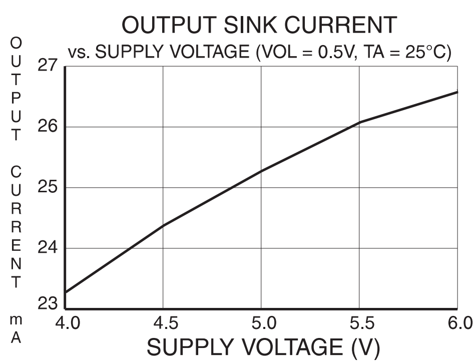
- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

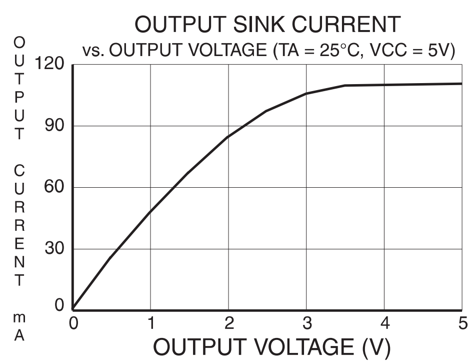

SUPPLY CURRENT vs. INPUT FREQUENCY
ATV750B (TA = 25°C, VCC = 5V)
ICC mA
150
125
100
75
50
25
0
ATV750B
0
10
20
30
40
50
FREQUENCY (MHz)

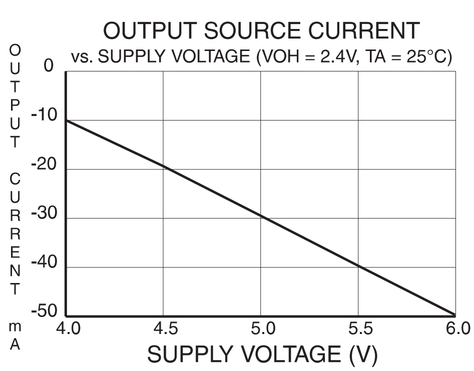

SUPPLY CURRENT vs. INPUT FREQUENCY
ATV750BL (TA = 25°C, VCC = 5V)
ICC mA
150
125
100
75
50
25
0
ATV750BL
0
15
30
45
60
75
FREQUENCY (MHz)

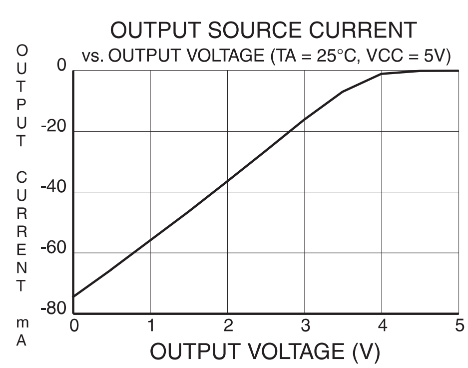

NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE (TA = 25°)
NORMALIZED ICC
1.8
1.4
1.0
0.6
0.2
4.0
4.5
5.0
5.5
6.0
SUPPLY VOLTAGE (V)


NORMALIZED ICC vs. AMBIENT TEMP.
(f = 50 MHz, VCC = 5V)
NORMALIZED ICC
1.15
1.05
0.95
0.85
-55
-25
5
35
65
95
125
AMBIENT TEMPERATURE (C)

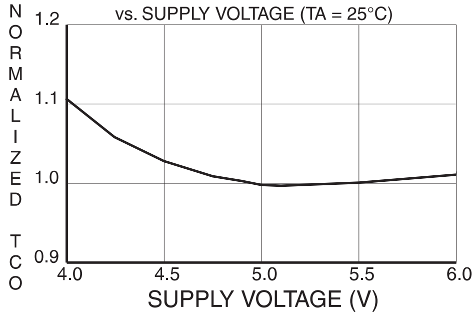

OUTPUT SINK CURRENT
vs. SUPPLY VOLTAGE (VOL = 0.5V, TA = 25°C)
OUTPUT CURRENT mA
27
26
25
24
23
4.0
4.5
5.0
5.5
6.0
SUPPLY VOLTAGE (V)


OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (TA = 25°C, VCC = 5V)
OUTPUT CURRENT mA
120
90
60
30
0
0
1
2
3
4
5
OUTPUT VOLTAGE (V)

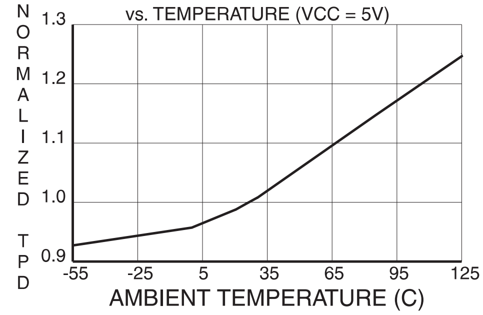

OUTPUT SOURCE CURRENT
vs. SUPPLY VOLTAGE (VOH = 2.4V, TA = 25°C)
OUTPUT CURRENT mA
0
-10
-20
-30
-40
-50
4.0
4.5
5.0
5.5
6.0
SUPPLY VOLTAGE (V)


OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (TA = 25°C, VCC = 5V)
OUTPUT CURRENT mA
0
-20
-40
-60
-80
0
1
2
3
4
5
OUTPUT VOLTAGE (V)

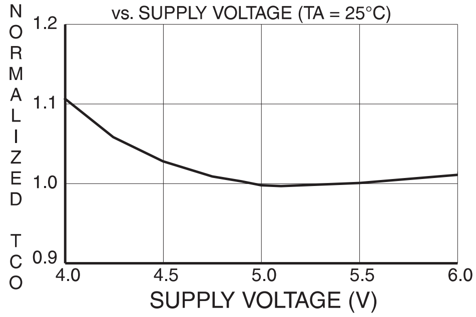
NORMALIZED t_{CO}
vs. SUPPLY VOLTAGE (TA = 25°C)



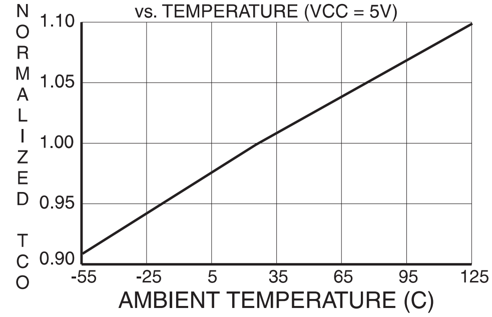
NORMALIZED t_{PD}
vs. TEMPERATURE (VCC = 5V)



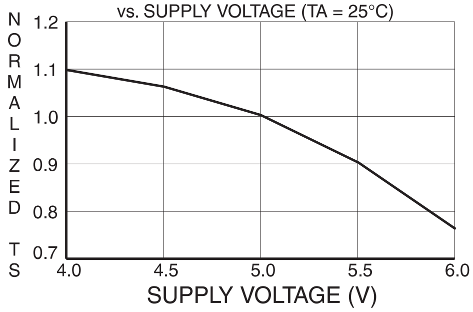
NORMALIZED t_{CO}
vs. SUPPLY VOLTAGE (TA = 25°C)



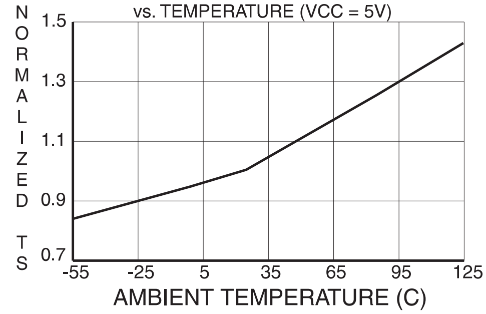
NORMALIZED t_{CO}
vs. TEMPERATURE (VCC = 5V)



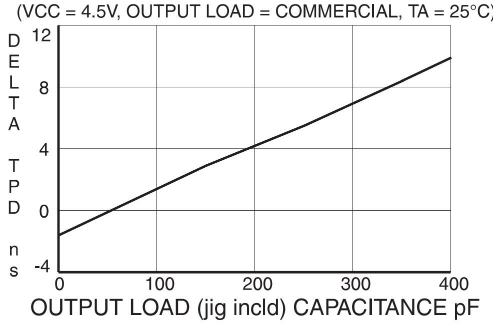
NORMALIZED t_S
vs. SUPPLY VOLTAGE (TA = 25°C)



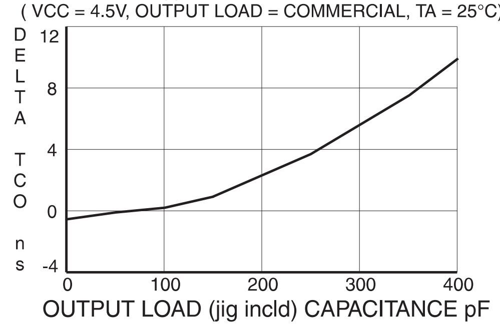
NORMALIZED t_S
vs. TEMPERATURE (VCC = 5V)



DELTA t_{PD} vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL, TA = 25°C)



DELTA t_{CO} vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL, TA = 25°C)



Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
7.5	6.5	95	ATV750B-7JC ATV750B-7PC	28J 24P3	Commercial (0°C to 70°C)
10	7	83	ATV750B-10JC ATV750B-10PC ATV750B-10SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-10JI ATV750B-10PI ATV750B-10SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750B-10DM/883 ATV750B-10LM/883	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	58	ATV750B-15JC ATV750B-15PC ATV750B-15SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-15JI ATV750B-15PI ATV750B-15SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750B-15DM/883 ATV750B-15LM/883	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	41	ATV750B-25JC ATV750B-25PC ATV750B-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-25JI ATV750B-25PI ATV750B-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
10	7	83	5962-88726 08 LA 5962-88726 08 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	9	58	5962-88726 09 LA 5962-88726 09 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

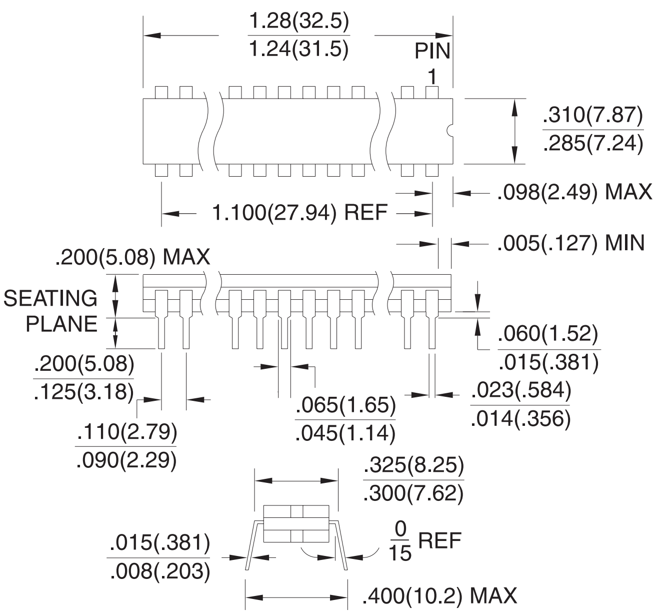
Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	9	92	ATV750BL-15JC ATV750BL-15PC ATV750BL-15SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750BL-15JI ATV750BL-15PI ATV750BL-15SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750BL-15DM/883 ATV750BL-15LM/883	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	37	ATV750BL-25JC ATV750BL-25PC ATV750BL-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750BL-25JI ATV750BL-25PI ATV750BL-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
15	9	92	5962-88726 11 LX 5962-88726 11 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

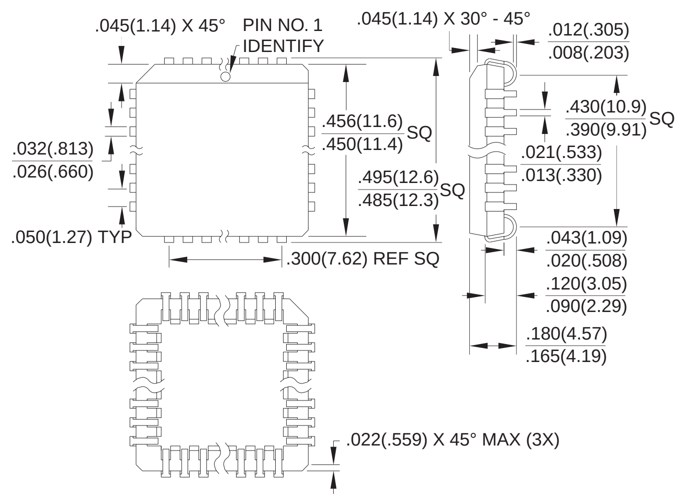
Package Type	
24DW3	24-Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28J	28-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24-Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

Packaging Information

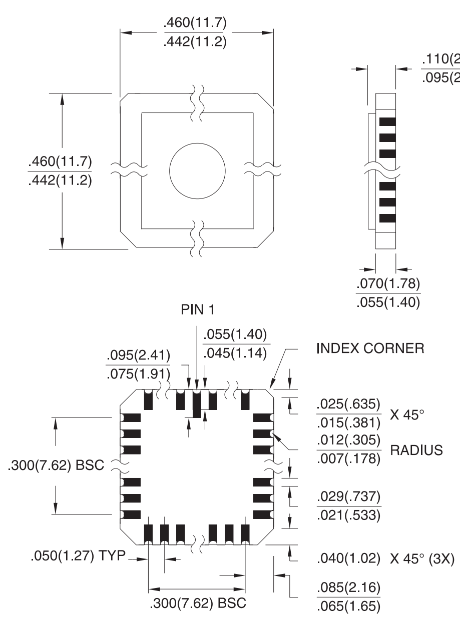
24DW3, 24-Lead, 0.300" Wide, WIndowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A



28J, 28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AB

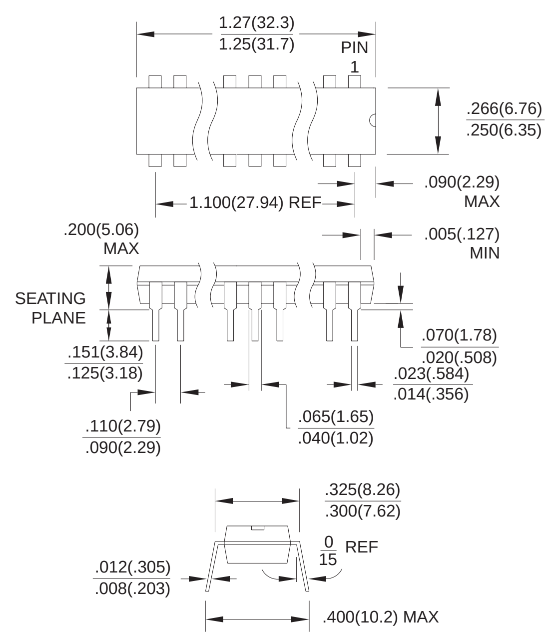


28LW, 28-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-4



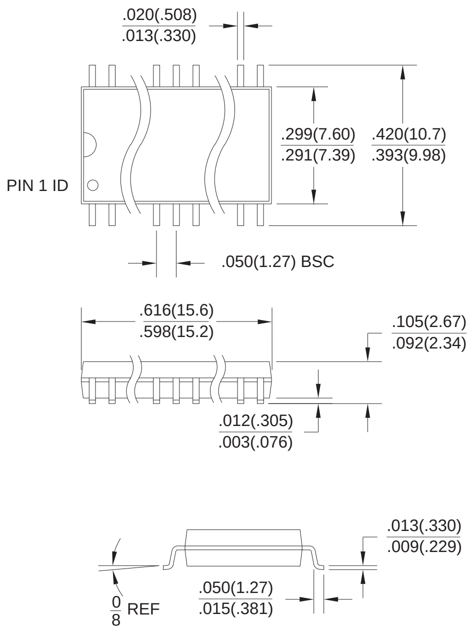
*Controlling dimension: millimeters

24P3, 24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AF



Packaging Information

24S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



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